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EXAMINER
ORTIZ, EDGARDO

ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/875,501	Applicant(s) Schuegraf Et.al.
	Examiner Edgardo Ortiz	Art Unit 2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Jul 8, 2002*

2a)☐ This action is **FINAL.** 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21, 22, and 29-41* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideratio

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21, 22, and 29-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examine

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some* c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a)☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 10 & 13
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This Office Action is in response to a Request for Continued Prosecution and amendment filed on July 8, 2002 on which Applicant amended claim 21 and added new claims 32-41.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 21, 29-34, 36-38, 40 and 41 are rejected under 35 U.S.C. § 102 (b) as being anticipated by Chen et.al. (U.S. Patent No. 5,472,896). With regard to Claim 21, Chen teaches a polysilicon layer (14), a metal-silicide layer (16) against the layer of polysilicon, the metal-silicide layer comprising a Group III or a Group V dopant (As) and a silicon-dioxide-containing dopant barrier layer (22) against the metal silicide layer, the metal-silicide layer comprising the only structure directly below and against the barrier layer. As clearly shown on figure 3f, the conductive line or gate stack portion of the semiconductor device that includes the polysilicon layer and the metal-silicide layer also includes a silicon-dioxide-containing dopant barrier layer over the metal-silicide layer, wherein the metal-silicide layer is "the only structure directly below and against the barrier layer" as claimed.

With regard to Claim 29, Chen teaches a silicon-dioxide-containing dopant barrier layer (22) that is elevationally above the metal-silicide layer (16).

With regard to Claim 30, Chen teaches a metal-silicide layer (16) that comprises an elevationally uppermost surface relative to the polysilicon layer (14), and wherein a silicon-dioxide-containing dopant barrier layer (22) is against the uppermost surface.

With regard to Claim 31, Chen teaches a metal-silicide layer (16) that comprises an elevationally uppermost surface relative to a polysilicon layer (14), the uppermost surface having a width dimension, and wherein a silicon-dioxide-containing dopant barrier layer (22) is against substantially the entire width of the uppermost surface.

With regard to Claim 32, Chen teaches a polysilicon layer (14), a metal-silicide layer (16) against the layer of polysilicon, a doped metal-silicide layer, a silicon-dioxide-containing dopant barrier layer (22) against the metal silicide layer and the polysilicon layer, the metal-silicide layer and barrier layer having aligned respective sidewalls, as shown on figure 3f, the aligned respective sidewalls defining an entirety of a lateral width for the conductive line.

With regard to Claim 33, Chen teaches a doped metal-silicide layer (16) comprising a Group III or a Group V dopant (As).

With regard to Claim 34, Chen teaches a silicon-dioxide-containing dopant barrier layer (22) that is against only the metal silicide layer in the conductive line or gate stack portion of the semiconductor device, as clearly shown on figure 3f.

With regard to Claim 36, Chen teaches a polysilicon layer (14) supported by a substrate (10), a doped metal-silicide layer (16) supported by the polysilicon layer and a silicon-dioxide-containing dopant barrier layer (22) elevationally over the metal-silicide layer and the substrate, the barrier layer is against the metal-silicide layer only, with respect to the substrate and the metal-silicide, as clearly shown on figure 3f.

With regard to Claim 37, Chen teaches a doped metal-silicide layer (16) comprising a Group III or a Group V dopant (As).

With regard to Claim 38, Chen a polysilicon layer (14) that comprises a lateral width that is substantially equal to a lateral width of the conductive line.

With regard to Claim 40, Chen teaches a metal-silicide layer (16) that comprises a lateral width that is substantially equal to a lateral width of the conductive line.

With regard to Claim 41, Chen teaches a silicon-dioxide-containing dopant barrier layer (22) that comprises a lateral width that is substantially equal to a lateral width of the conductive line.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 22, 35 and 39 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Chen et.al. (U.S. Patent No. 5,472,896) in view of Ilg et al. (U.S. Patent No. 6,130,145). Chen, as stated supra, essentially disclose the claimed invention but fail to show, a concentration of dopants in the metal-silicide layer of at least 1 x 10E18 ions/cubic cm. With regard to Claims 22, 35 and 39; Ilg discloses an insitu doped metal polycide which includes a polysilicon layer (230) and a metal-silicide layer (240) against the layer of polysilicon, wherein the metal-silicide layer comprises a Group III dopant (B) or a Group V dopant (P, As) and has a concentration of dopants of at least 1 x 10E18 ions/cubic centimeter. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Chen to include a metal-silicide layer with a concentration of dopants of at

least 1 x 10E18 ions/ cubic cm in a gate structure, as clearly suggested by Ilg, in order to lower the resistance of the metal-silicide layer.

Claims 21, 22 and 29-41 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Kuroda (U.S. Patent No. 5,986,312) in view of Ilg et al. (U.S. Patent No. 6,130,145). With regard to Claim 21, Kuroda teaches a polysilicon layer (14), a metal-silicide layer (33) against the layer of polysilicon and a silicon-dioxide-containing dopant barrier layer (34) against the metal-silicide layer, wherein the metal-silicide layer comprises the only structure directly below and against the barrier layer, as clearly shown on figure 2.

However, Kuroda fails to teach that the metal-silicide layer comprises a Group III or Group V dopant. Ilg teaches an insitu doped metal polycide which includes a polysilicon layer (230) and a metal-silicide layer (240) against the layer of polysilicon, wherein the metal-silicide layer comprises a Group III dopant (B) or a Group V dopant (P, As). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Kuroda to include the metal-silicide layer comprising a Group III or Group V dopant, as clearly suggested by Ilg, in order to lower the resistance of the metal-silicide layer.

With regard to Claim 22, a further difference between the claimed invention and Kuroda is, a doped concentration of 1 x 10E18 ions/cm3. Ilg discloses an insitu doped metal polycide which includes a polysilicon layer (230) and a metal-silicide layer (240) against the layer of polysilicon, wherein the metal-silicide layer comprises a Group III dopant (B) or a Group V dopant (P, As) and has a concentration of dopants of at least 1 x 10E18 ions/cubic centimeter. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Kudora to include a metal-silicide layer with a concentration of dopants of at least 1 x 10E18 ions/ cubic cm in a gate structure, as clearly suggested by Ilg, in order to lower the resistance of the metal-silicide layer.

With regard to Claim 29, Kuroda teaches a silicon-dioxide-containing dopant barrier layer (34) that is elevationally above the metal-silicide layer (33).

With regard to Claim 30, Kuroda teaches a metal-silicide layer (33) that comprises an elevationally uppermost surface relative to the polysilicon layer (14), and wherein a silicon-dioxide-containing dopant barrier layer (34) is against the uppermost surface.

With regard to Claim 31, Kuroda teaches a metal-silicide layer (33) that comprises an elevationally uppermost surface relative to a polysilicon layer (14), the uppermost surface having

a width dimension, and wherein a silicon-dioxide-containing dopant barrier layer (34) is against substantially the entire width of the uppermost surface.

With regard to Claim 32, Kuroda teaches a polysilicon layer (14), a metal-silicide layer (33) against the layer of polysilicon, a metal-silicide layer, a silicon-dioxide-containing dopant barrier layer (34) against the metal silicide layer and the polysilicon layer, the metal-silicide layer and barrier layer having aligned respective sidewalls, as shown on figure 2, the aligned respective sidewalls defining an entirety of a lateral width for the conductive line.

However, Kuroda fails to teach that metal-silicide layer is doped. Ilg teaches an insitu doped metal polycide which includes a polysilicon layer (230) and a metal-silicide layer (240) against the layer of polysilicon, wherein the metal-silicide layer comprises a Group III dopant (B) or a Group V dopant (P, As). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Kuroda to include the metal-silicide layer that is doped, as clearly suggested by Ilg, in order to lower the resistance of the metal-silicide layer.

With regard to Claim 33, a further difference between the claimed invention and Kuroda is, a doped metal-silicide layer (16) comprising a Group III or a Group V dopant (As). Ilg teaches an insitu doped metal polycide which includes a polysilicon layer (230) and a metal-silicide layer

(240) against the layer of polysilicon, wherein the metal-silicide layer comprises a Group III dopant (B) or a Group V dopant (P, As). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Kuroda to include the metal-silicide layer comprising a Group III or Group V dopant, as clearly suggested by Ilg, in order to lower the resistance of the metal-silicide layer.

With regard to Claim 34, Kuroda teaches a polysilicon layer (14), a metal-silicide layer (33) against the layer of polysilicon and a silicon-dioxide-containing dopant barrier layer (34) against the metal-silicide layer, wherein the metal-silicide layer comprises the only structure directly below and against the barrier layer, as clearly shown on figure 2.

With regard to Claim 35, a further difference between the claimed invention and Kuroda is, a doped concentration of 1 x 10E18 ions/cm3. Ilg discloses an insitu doped metal polycide which includes a polysilicon layer (230) and a metal-silicide layer (240) against the layer of polysilicon, wherein the metal-silicide layer comprises a Group III dopant (B) or a Group V dopant (P, As) and has a concentration of dopants of at least 1 x 10E18 ions/cubic centimeter. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Kudora to include a metal-silicide layer with a concentration of dopants of at least 1 x 10E18 ions/ cubic cm in a gate structure, as clearly suggested by Ilg, in order to lower the resistance of the metal-silicide layer.

With regard to Claim 36, Kuroda teaches a polysilicon layer (14) supported by a substrate (11), a metal-silicide layer (33) supported by the polysilicon layer and a silicon-dioxide-containing dopant barrier layer (22) elevationally over the metal-silicide layer and the substrate, and the barrier layer is against only the metal-silicide layer with respect to the substrate and the metal-silicide.

However, Kuroda fails to teach that the metal-silicide layer is doped. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Chen to include the barrier layer is against the metal-silicide layer only, with respect to the substrate and the metal-silicide, as clearly suggested by Kuroda, in order to permit the implantation of dopants in other regions of the semiconductor device, for example, to create lightly doped diffusion regions.

With regard to Claim 37, a further difference between the claimed invention and Kuroda is, a doped metal-silicide layer (16) comprising a Group III or a Group V dopant (As). Ilg teaches an insitu doped metal polycide which includes a polysilicon layer (230) and a metal-silicide layer (240) against the layer of polysilicon, wherein the metal-silicide layer comprises a Group III dopant (B) or a Group V dopant (P, As). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Kuroda to include the metal-silicide layer comprising a Group III or Group V dopant, as clearly suggested by Ilg, in order to lower the resistance of the metal-silicide layer.

With regard to Claim 38, Kuroda a polysilicon layer (14) that comprises a lateral width that is substantially equal to a lateral width of the conductive line.

With regard to Claim 39, a further difference between the claimed invention and Kuroda is, a doped concentration of 1 x 10E18 ions/cm3. Ilg discloses an insitu doped metal polycide which includes a polysilicon layer (230) and a metal-silicide layer (240) against the layer of polysilicon, wherein the metal-silicide layer comprises a Group III dopant (B) or a Group V dopant (P, As) and has a concentration of dopants of at least 1 x 10E18 ions/cubic centimeter. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Kudora to include a metal-silicide layer with a concentration of dopants of at least 1 x 10E18 ions/ cubic cm in a gate structure, as clearly suggested by Ilg, in order to lower the resistance of the metal-silicide layer.

With regard to Claim 40, Kuroda teaches a metal-silicide layer (33) that comprises a lateral width that is substantially equal to a lateral width of the conductive line.

With regard to Claim 41, Kuroda teaches a silicon-dioxide-containing dopant barrier layer (34) that comprises a lateral width that is substantially equal to a lateral width of the conductive line.

Response to Arguments

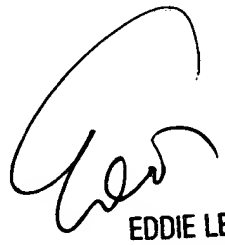
3. Applicant's arguments with respect to claims 21, 22 and 29-41 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Edgardo Ortiz (Art Unit 2815), whose telephone number is (703) 308-6183. In case the Examiner can not be reached by a direct telephone call, you might call Supervisor Eddie Lee at (703) 308-1690. Any inquiry of a general nature or relating to the status of this application should be directed to the Group 2800 receptionist whose telephone number is (703) 308-0956.

EO / AU 2815

8/23/02



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